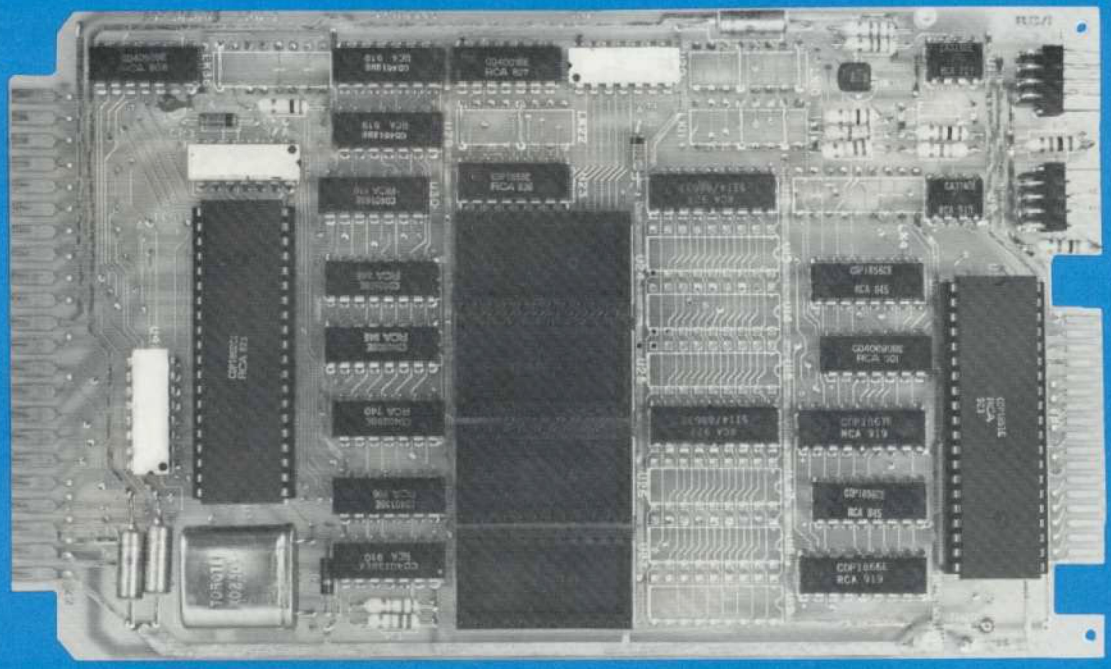
RCA Solid State

RCA Microboard Computer

CDP18S603A



RCA Microboard
Milliwatt Computer Systems

MB-603A

RCA Microboard Computer

CDP18S603A

The RCA Microboard Computer CDP18S603A is a versatile computer system on a single 4.5 x 7.5 inch card. The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power-on reset, and expansion interface. Four on-board sockets are provided for read-only memory enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. The CDP18S603A Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and special requirements of his specific application.

The CDP18S603A is plug-in compatible with the RCA MSI Series of Industrial Chassis and with RCA Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 and Color CMCDS CDP18S695 to facilitate hardware and software development. It can also be used with RCA Prototyping Systems CDP18S691 and CDP18S692, and RCA Development Systems CDP18S005 (CDSII) and CDP18S007 (CDSIII).

Features

- **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Current required — 7 to 27 mA (typ.)†**
- **High noise immunity**
- **2-MHz crystal clock**
- **Compatible with RCA MSI Series of Industrial Chassis, and RCA 1800-Series Development Systems**
- **Stand-alone capability**
- **1 kilobyte of read/write memory**
- **Sockets for 4/8 kilobytes of ROM/PROM**
- **Power-on reset**
- **1800-Series Microprocessor architecture**
- **Flexible memory and I/O expansion**
- **20 programmable parallel I/O lines**
- **4 flag inputs**
- **Q serial data output**
- **RS232C or 20-mA serial I/O**
- **65,536-byte memory space**
- **44-pin system interface**
- **Wide temperature range: -40° C to 85° C**
- **Small board size — 4.5 x 7.5 inches**

†Depending whether 20-mA serial interface is used.

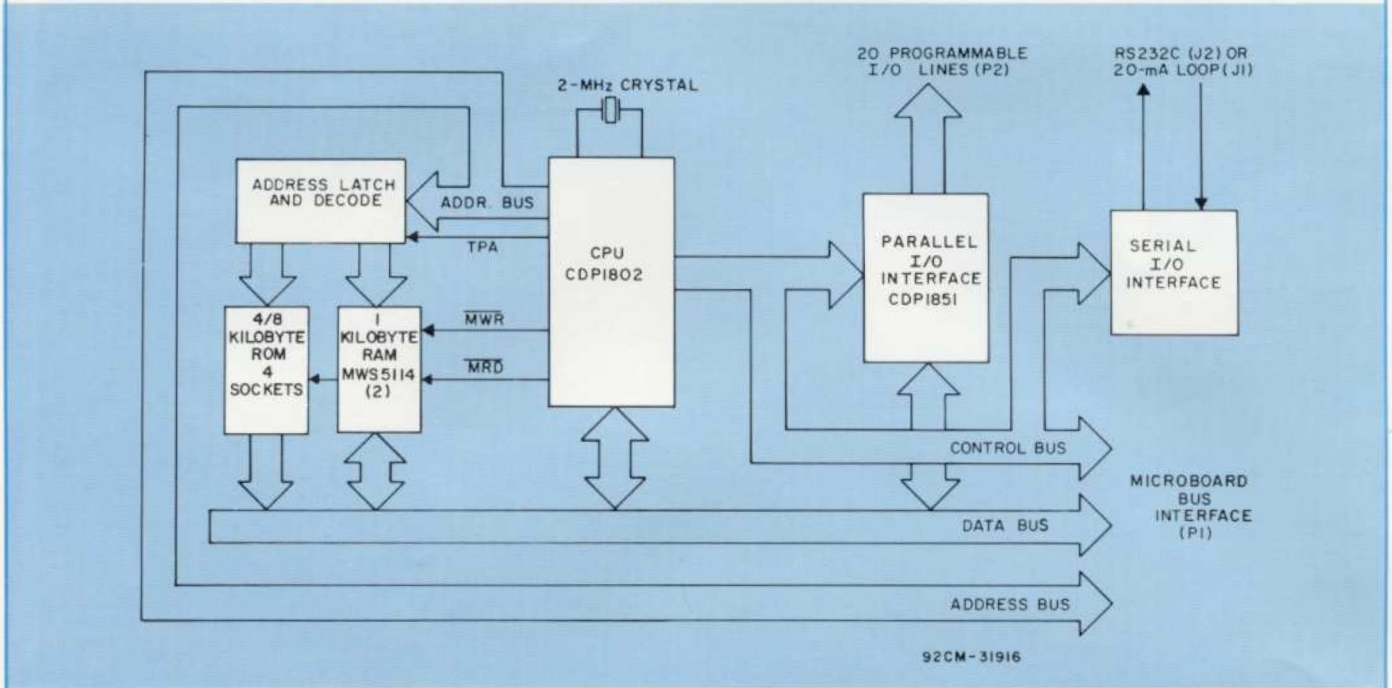


Fig. 1 — Block diagram of RCA Microboard Computer CDP18S603A.

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Printed in USA/9-82
Supersedes MB603
Issued 11/80

Component Features

Central Processing Unit. The central processor for the CDP18S603A Microboard Computer is the 8-bit silicon-gate CMOS RCA Microprocessor CDP1802. The CDP-1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

Memory. By means of two MWS5114 RAM's, the CDP18S603A provides 1 kilobyte of CMOS read-write memory. Four sockets are provided for four or eight kilobytes of non-volatile read-only memory. RCA CDP-1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one-kilobyte boundaries.

I/O. By means of the CMOS programmable I/O Interface CDP1851, the CDP18S603A provides twenty programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique "handshaking" signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. Right-angle header connections are provided for the serial communications interfaces.

Application

The RCA Microboard Computer CDP18S603A may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or the parallel I/O connector or wired directly to the board.

The CDP18S603A may be conveniently operated in conjunction with other Microboard Systems Components in the MSI Series of Industrial Chassis.

It may also be operated in conjunction with other Microboard System components installed in any location in the five-card Microboard Chassis (CDP18S675) or in the 22-card Microboard Chassis (CDP18S670). No link changes are required.

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

Specifications

Memory Capacity

On-board RAM: 1 kilobyte

On-board ROM/EPROM: 4 sockets for up to 8 kilobytes.

Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM.

Memory Address Map

On-board RAM: Low 1-kilobyte block in any 4-kilobyte block.

On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block.

I/O Capacity

Parallel: 20 lines each programmable as input, output, or bidirectional.

Serial: One input, one output, choice of 20-mA loop or RS232C. User-programmed baud rate and format.

Operating Temperature Range

–40°C to +85°C

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm)

Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements

Without ROM's, using RS232C: +5V (typical),

4.3 mA in WAIT or RESET MODE

6.5 mA operating with all memory access off-board.

41.0 mA with every machine cycle an on-board RAM access.

Optional voltages used only for RS232C interface:

+12 to +15 V at 8 mA, typical

–5 to –15 V at 8 mA, typical

Connectors

System Interface: Edge fingers, 44 pins on 0.156-inch centers.

Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.

Serial I/O: Two right-angle headers, 10 pin.

Clock

CPU and Interface: 2-MHz crystal-controlled oscillator on CPU.

RCA Microboard Computer
CDP18S603A

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the RCA Microboard Computer CDP18S603A and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1802 (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201. These signals are summarized in Table IX which gives a list of the pins and the signals for the RCA Universal Backplane Connector (P1).

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{MRD}$ line. When high, $\overline{MRD}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$ — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The CDP18S603A uses EF1 and EF2, conditioned by the secondary I/O address, to test the READY state of I/O ports A and B. The serial data interface input is presented directly on EF4 and EF3 chosen by link LK36. I/O devices using the INT line may make use of the EF lines to identify the device. They may also be used to indicate priority or status.

$\overline{INT}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of INT results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

$\overline{DMAI}$, $\overline{DMAO}$ — Taken directly to the CPU pins and not utilized by the CDP18S603A, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S603A buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{MWR}$ — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{MRD}$ — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR

must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless MRD is properly used to condition data output.

Q — A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions. The CDP18S603A may use Q as a serial data output to the RS232C and 20-mA data terminal drivers. It is also available for other uses through the Microboard Bus (P1) and Parallel I/O (P2) connectors. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT — A 2-MHz square-wave clock provided for general use. It is derived from the crystal-controlled oscillator in the CPU.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ — Two control inputs to the CPU which determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load Mode. Holds the CPU in the IDLE state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that termination of the DMA-IN operation does not force execution of the next instruction. DMA-IN requests then load memory starting from location zero for as many bytes as there are DMA-IN requests.

Reset Mode. Registers I, N, and Q are reset, IE is set, and 0's (Vss) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, and registers X, P, and R0 are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2, but never an S3. Power-up reset is obtained by a Schmitt-trigger buffered RC network connected to $\overline{\text{CLEAR}}$.

Pause Mode. Stops the internal CPU timing generator on the first high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run Mode. May be initiated from the Pause or Reset Mode functions. If initiated from Pause, the CPU resumes operation on the first high-to-low transition of the input clock. If initiated from Reset, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to the CDP18S603A to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address. The RAM on the CDP18S603A is 4 kilobytes of contiguous memory. The high-order four bits of memory address are latched and decoded, and a set of eight links is provided so that any value of the four high-order bits may be selected as the address of this RAM. Thus, the RAM may occupy 1 kilobyte starting at any even 4-kilobyte block in the memory space. Because the 4-kilobyte decoder enables the data buffers U5 and U8, the whole 4-kilobyte block selected for RAM is removed from the available memory space.

To set up the RAM address, install two jumpers in link LK11, according to Table I. Alternatively, a DIP switch may be installed if frequent changes are anticipated.

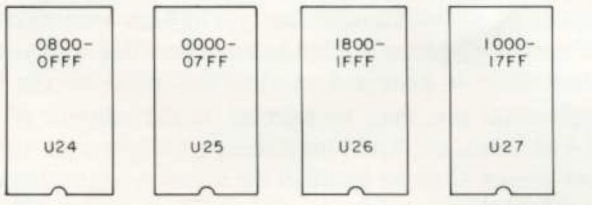
ROM Address. Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). The CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM chips may be used.

Two types of links are provided and must be made up by the user to suit the particular ROM configuration selected. The first link type is for accommodating the type

Table I — 4-Kilobyte Link Connections

4-Kilobyte Address Space	Link LK10, LK11, or LK22 Pin Connections
0000-0FFF	1:16, 5:12 †ROM LK10
1000-1FFF	1:16, 6:11 †ROM LK22
2000-2FFF	1:16, 7:10
3000-3FFF	1:16, 8:9
4000-4FFF	2:15, 5:12 †RAM LK11
5000-5FFF	2:15, 6:11
6000-6FFF	2:15, 7:10
7000-7FFF	2:15, 8:9
8000-8FFF	3:14, 5:12
9000-9FFF	3:14, 6:11
A000-AFFF	3:14, 7:10
B000-BFFF	3:14, 8:9
C000-CFFF	4:13, 5:12
D000-DFFF	4:13, 6:11
E000-EFFF	4:13, 7:10
F000-FFFF	4:13, 8:9

LINK 11 is associated with the 4-kilobyte RAM.
LINK 10 is associated with the ROM sockets 25 and 24.
LINK 22 is associated with the ROM sockets 27 and 26.
To defeat the RAM or either bank of ROM sockets, remove the jumpers in the associated link (11, 10, or 22) and on that link ground pins 9 and 6.
†Pre-linked



Prelinked 2K x 8 ROM Address Layout

of ROM selected (CDP1834, 2708, 2758, or 2716). The second link type is for selecting the memory address space to be occupied by the ROM.

Link LK4 is an 18-pin dual-in-line arrangement with preprinted links to accomodate the 2716. Table II gives the connections required for each ROM type.

Links LK10 and LK22 are 16-pin dual-in-line arrangements with no preprinted links. A DIP switch may be installed if frequent address changes are expected. Link LK10 provides the high-order four address bits decoded so that two links or jumpers place sockets XU24 and XU25 in any 4-kilobyte block within the 64-kilobyte memory address space. Link LK22 does the same for sockets XU26 and XU27. See Table I for address map and link connections.

To avoid having floating inputs to the gates, both links LK10 and LK22 should always have two jumpers. For example, if sockets XU26 and XU27 are unused, LK22 may be jumpered the same as LK10. Otherwise, spurious chip selects may be generated, turning on the three-state data buffers and causing interference with normal processing.

In instances where the ROM sockets are not fully occupied, it may be desirable to jumper links LK10 or LK22, or both, identically with LK11 so that the unused ROM space overlays the RAM space. Although the 1-kilobyte RAM usurps the whole of its 4-kilobyte assignment on LK11, the remaining 3 kilobytes may be filled by (1) leaving socket XU25 empty; (2) populating sockets XU24, XU26, and XU27 with 1 kilobyte devices; and (3) jumpering LK10, LK11, and LK22 identically. If there is to be no ROM on this board, this linking will prevent the unused sockets from being assigned to memory space perhaps needed by other system boards.

For 1-kilobyte ROM's such as the CDP1834, 2708, or 2758, links LK10 and LK22 should be jumpered identically in accordance with Table I. Then, the ROM's should be installed in sockets XU25, XU27, XU24, and XU26, in that order, starting with the lowest-address ROM.

For 2-kilobyte ROM's (2716), links LK10 and LK22 should be jumpered independently in accordance with Table I for the required two 4-kilobyte blocks. Then, socket XU25 is the low 2 kilobytes and socket XU24 is the high 2 kilobytes of the 4-kilobyte block as set in LK10. Similarly, socket XU27 is the low 2 kilobytes and socket XU26 is the high 2 kilobytes of the 4-kilobyte block set in LK22.

One-kilobyte ROM type CDP1834 is the only one that may be used in combination with two-kilobyte ROM's type 2716. If all links are set up for the 2-kilobyte ROM's as shown in Table II for LK4, and LK10 and LK22 are set up for different 4-kilobyte blocks, then a 1-kilobyte ROM in socket XU25 will occupy the two lower 1-kilobyte segments of the 4-kilobyte block. In other words, its 1 kilobyte will "wrap" through the lower 2 kilobytes of the 4-kilobyte block. If it is in socket XU24, it will wrap through the upper 2 kilobytes of the 4-kilobyte block. A 2-kilobyte ROM may be placed in either socket XU24 or socket XU25 while the other is occupied by a 1-kilobyte ROM. Socket XU27 (low 2 kilobytes) and socket XU26 (high 2 kilobytes) may be used in the same manner.

Table II — ROM Type Selection Links

Link LK4 Pins	ROM Type			
	CDP1834	2708	2758	2716*
1:18	X	OPEN	SHORTED	SHORTED
2:17	X	SHORTED	OPEN	OPEN
3:16	SHORTED	SHORTED	SHORTED	OPEN
4:15	OPEN	OPEN	OPEN	SHORTED
5:14	OPEN	OPEN	OPEN	SHORTED
6:13	SHORTED	SHORTED	SHORTED	OPEN
7:12	X	SHORTED	OPEN	OPEN
8:11	X	OPEN	OPEN	SHORTED
9:10	X	OPEN	SHORTED	OPEN

X = don't care; *Link LK4 is prewired to accept 2716.

I/O Operation

Serial I/O Interface. Serial data output is generated by the Q line from the CPU. Thus, software using the SET Q and RESET Q instructions generates data rate and format. Serial data input is presented to either EF3 or EF4, selectable by links as shown in Table III. The software uses the test branch instructions to decode incoming data.

Table III — Link Table for Serial Data In

Link LK36	Function
7:10	Data to EF3
8:9	Data to EF4

Electrical interfaces for either the 20-mA loop or RS232C data terminals are provided on connectors J1 and J2 respectively. Output drivers are separate but the input receiver is shared. The only modification required for RS232C interface is the installation of a jumper wire in the C5 holes. RS232C data terminals require that +12 volts be available on pin 20 of the backplane and –5 volts be available on pin 11.

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S603A does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The CDP18S603A uses bit three as the group select; that is, the group number $(08)_{16}$ or $(0000\ 1000)_2$ is transmitted by the 61 output instruction to select the programmable I/O on board.

In general, although Interrupt is not gated by group select, External Flags are gated by the appropriate group select. The serial interface on the CDP18S603A, however, uses either EF3 and EF4 with no gating by group number. Therefore, when the serial interface is wired for use, EF3 or EF4, whichever was chosen, is not generally available for other devices.

Parallel I/O Interface. The parallel I/O interface consists of 20 lines provided on connector P2. These 20 lines are generated by the CDP1851 Programmable I/O Interface and may be programmed as input, output, or bidirectional individually or as a block. The P2 connector also provides the Q line, EF1 through EF4, CLEAR, three different voltages, and a logic ground.

For more detailed information on the Programmable I/O Interface CDP1851, refer to the data sheet for that device. (File No. 1056).

The CDP1851 is assigned to I/O group eight. Therefore, in order to enable access, a 61 output instruction with data = 08 is required before read, write, or control I/O may be performed.

Signal ARDY conditioned by the group select gener-

ates EF1; BRDY and group select generates EF2. Link LK41, pins A and B may be jumpered if interrupt-driven software is to be used. Then, INTA or INTB generates INT unconditionally.

Once the group select is accomplished, N1 and N2 are used to address the CDP1851. The following read and write instructions are used to access data, status, and command registers.

62 or 63 — Write to control register
64 or 65 — Write to Port A data register (if A is an output)
66 or 67 — Write to Port B data register (if B is an output)
6A or 6B — Read status register
6C or 6D — Read Port A data register (if A is an input)
6E or 6F — Read Port B data register (if B is an input)

Using the READY Lines for Data Synchronization. The Port A and Port BRDY lines are presented to the CPU EF1 and EF2 lines when the group select is set. Even though these RDY lines are primarily intended for "handshaking" with the device on the other end of the cable, they are useful for synchronizing data transfer between the CDP1851 and the CPU. Note that there is a logic reversal: when RDY is true, the EF is false. Because of the logic reversal and because the event of interest is RDY going false, the EF true test is used. A test for ARDY might use the B1 instruction (34) which would take the branch if ARDY were false.

When a port designated as an **output** port is loaded, RDY goes true. When the receiving device takes the data, it transmits STB which removes RDY. The software can then test RDY until it is false (EF1 and EF2 true), and load the next output byte. When a port is designated as an **input** port, reading the data sets RDY, and the transmitting device resets RDY when it transmits data and STB. Again, the software tests to see if RDY is false and then reads the input byte. **In this case, a dummy read after reset is necessary to raise the first RDY.**

Note that if the remote device is passive, such as a display or a set of points, handshaking is not necessary. The output port may be loaded at any time to change data without acknowledgment from the remote device. Similarly, the input port may be read at any time to store the current state of the input lines.

Using the INTERRUPT Line for Data Synchronization. If link LK41, A:B is jumpered, INTA or INTB generates INT to the CPU. INT is not conditioned by the group select. INT is set by the remote device sending STB to acknowledge an output port and is reset by loading an output port. Similarly, INT is set by the remote device sending STB to load an input port and is reset by reading the input port. Table IV summarizes the actions of READY and INT for input and output modes.

The software can find the source of the interrupt by setting the group select 08, and then, either testing the RDY lines or reading the status byte. The low-order two bits of the status byte are: bit 0 = INTB; bit 1 = INTA.

Bidirectional Mode. Port A may be programmed to be bidirectional. In this case, Port B must be programmed to be in the bit-programmable mode, to be described later. In the bidirectional mode, ARDY and ASTB become A INPUT RDY and A INPUT STB; BRDY becomes A OUTPUT RDY, and BSTB becomes A OUTPUT STB. Each of the eight lines AD0—AD7 may transmit data in both directions, using the input handshaking lines to synchronize inputs and the output handshaking lines for the output data. Operation is much the same as for independent input and output ports except that output data is gated into AD0-AD7 only when the OUTPUT STB line is raised. In summary, Port A in the bidirectional mode is an output port and an input port sharing the same eight data lines, each having a set of handshaking lines.

Bit-Programmable Mode. Both Port A and Port B are capable of being programmed to be in the bit-programmable mode. Port B must be in this mode if Port A is in the bidirectional mode. In the bit-programmable mode, each line in AD0-AD7 and B0-B7 is programmed to be either input or output. In addition, the handshaking lines are programmed to be input or output lines unless Port A is bidirectional, in which case it uses all four

Table IV — READY and INTERRUPT Actions for Input and Output Modes.

		Output Port	Input Port
READY	Set by	Loading Data	Reading Data
	Reset by	STB leading edge	STB leading edge
INTERRUPT	Set by	STB trailing edge	STB trailing edge
	Reset by	Loading Data	Reading Data

handshaking lines. The handshaking lines, when used as data lines, are accessed by a write control for output lines and read status for input lines. The other eight lines in each port are accessed by the usual read and write data instructions.

Interrupts are generated when an input line goes true except that the former handshaking lines cannot generate interrupts. The bits may be individually masked so as not to generate interrupts. The interrupt control word selects one of the two interrupt rules, AND or OR. The AND rule results in an interrupt only when all unmasked lines are true. The OR rule results in an interrupt when any unmasked line is true. The interrupt control word also defines the input lines as logically true when high or logically true when low.

Power-On Reset

An RC integrator (R1 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U30) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, and the I/O group-select latch. After the CLEAR signal, the I/O group select is reset, the parallel I/O interface Ports A and B are set to be input ports, the mask register is reset (monitors all bits), and the status register is reset. The CPU initializes and starts processing at location 0000 (provided the WAIT line is not asserted).

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the RCA Development Systems CDP18S005 (CDS II) or CDP18S007 (CDS III)

Replacement of the CDS CPU Module CDP18S102 with the RCA Microboard Computer CDP18S603A requires some link changes on the CDP18S603A and wiring changes on the CDS backplane. These changes are:

LK43 — Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter and 2708 EPROM's), do not install A:D. See Table V.

Table V — Changes on Link LK43 for Installation of CDP18S603A in Development Systems CDP18S005 and CDP18S007.

LK43	A:B	C:D	A:D	B:C
Microboard	*Closed	*Closed	Open	Open
CDS	Open	Open	Closed	Closed

*Preprinted links

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK36 — Serial Data In to external flag lines. In the CDS II, if the Terminal Interface Module CDP18S507 is not retained, connect pins 8:9 for EF4 to make the CDP18S603A the operator's terminal interface. If the CDP18S507 is retained, EF3 may be used for another serial interface purpose by connecting pins 7:10. In the CDS III, the UART module in location 14 is the operator's terminal interface and pins 7:10 and 8:9 may be left open.

LK36 — RNU to start ROM's at address 8000. Cut the wire jumper in pins 5:12. If the RAM or ROM occupies memory address 0000 or if the ROM occupies memory address 8000 and is the monitor or utility program, install pins 6:11. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after RESET, RUNU switches are pressed. This wire should be removed when the CPU Module CDP18S102 is re-installed. See Table VI.

Table VI — Changes on Link LK36 for Installation of CDP18S603A in Development Systems CDP18S005 and CDP18S007.

LK36	RNU 5:12	RNU 6:11	EF3 7:10	EF4 8:9
Microboard	¢Closed	Open	Open	¢Closed
CDS	Open	Closed	Open	Closed@

¢Wire jumpers installed
@Assumes the CDP18S603A serial interface is to be the operator terminal interface

LK10, 11, and 22 — Set up as previously described for the memory address desired, taking care that the CDS memories are not assigned to overlap the assignment of the CDP18S603A Microboard Computer.

Table VII summarizes the required CDS backplane wiring changes.

Table VII — Summary of Backplane Wiring Additions Needed When the CDP18S603A is Installed in the Development Systems CDP18S005 and CDP18S007.

From		To		
Slot	Pin	Slot	Pin	Function
12	X	13	20	−12 V
12	11	14	11	−5 V
12	12	10	D	RNU-P†

†This connection should be removed when the CDP18S102 is reinstalled

Table VIII — List of Links and Their Functions

LK4	ROM Type Selection
*1:18	ROM Type 2758, 2716
2:17	ROM Type 2708
3:16	ROM Type 2758, 2708, or CDP1834
*4:15	ROM Type 2716
*5:14	ROM Type 2716
6:13	ROM Type 2758, 2708, or CDP1834
7:12	ROM Type 2708
*8:11	ROM Type 2716
9:10	ROM Type 2758

LK10	ROM Decoding for XU24 and XU25
¢1:16	$\overline{A15}$•$\overline{A14}$
2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
¢5:12	$\overline{A13}$•$\overline{A12}$
6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12

LK11	RAM Decoding
1:16	$\overline{A15}$•$\overline{A14}$
¢2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	$\overline{A15}$•A14
¢5:12	$\overline{A13}$•$\overline{A12}$
6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12

LK22	ROM Decoding for XU26 and XU27
¢1:16	$\overline{A15}$•$\overline{A14}$
2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
5:12	$\overline{A13}$•$\overline{A12}$
¢6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12

LK36	
1:16	Not applicable to CDP1802
*2:15	CLEAR-N
3:14	Not applicable to CDP1802
*4:13	WAIT-N
¢5:12	RNU-P from P1-3
6:11	RNU-P from P1-12 (CDS installation only)
7:10	EF3 for serial interface in
¢8:9	EF4 for serial interface in

LK37	
*A:B	+5 V V_{DD} to CDP1802

LK41	
A:B	Interrupt from PIO

LK43	
*A:B	Microboard system installation (EF4-N)
*C:D	Microboard system installation (+12 V)
A:D	CDS installation (+12 V)
B:C	CDS installation (EF4-N)

*Preprinted links ¢Wire jumpers installed

Table IX — Pin Terminals and Signals for the RCA Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow†	Description	Pin	Mnemonic	Signal Flow†	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	—	+5 V dc	21	+5 V	—	+5 V dc
Z	GND	—	Digital Ground	22	GND	—	Digital Ground

†Signal flow is with respect to CPU board.

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Table X
Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+ 5V
31	EF2-N	32	− 5V/ − 15V
33	EF1-N	34	+ 12V/ + 15V

Table XI
Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

RCA Microboard Computer
CDP18S603A

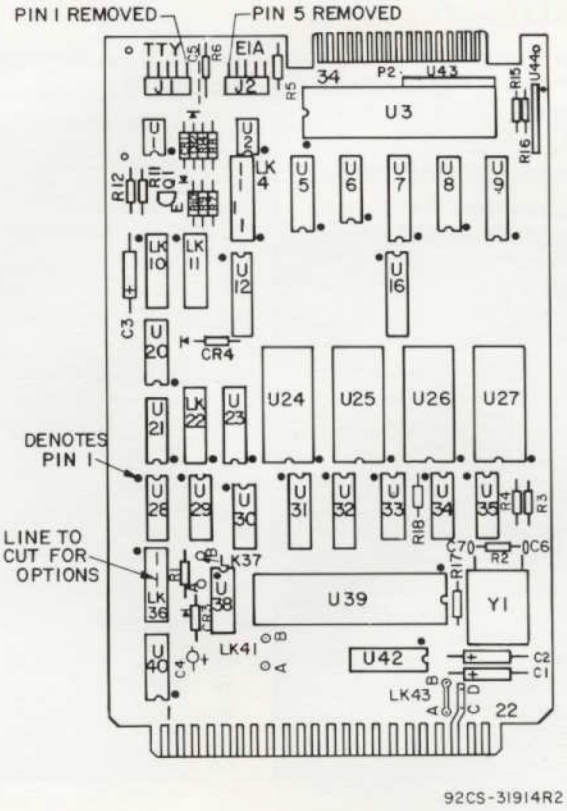

Fig. 2 — Layout diagram of RCA Microboard Computer CDP18S603A.

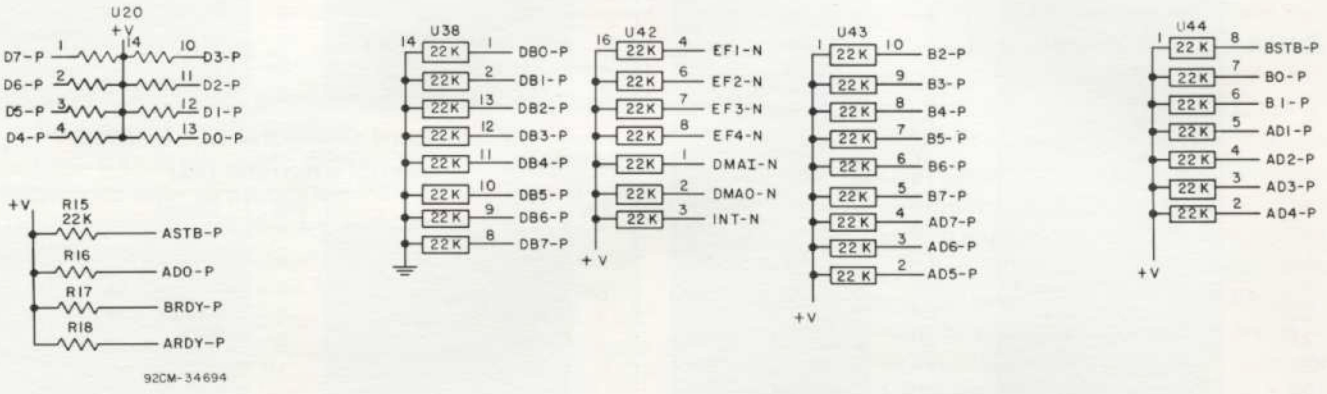

Fig. 3 — Pull-Down and Pull-Up Resistors.

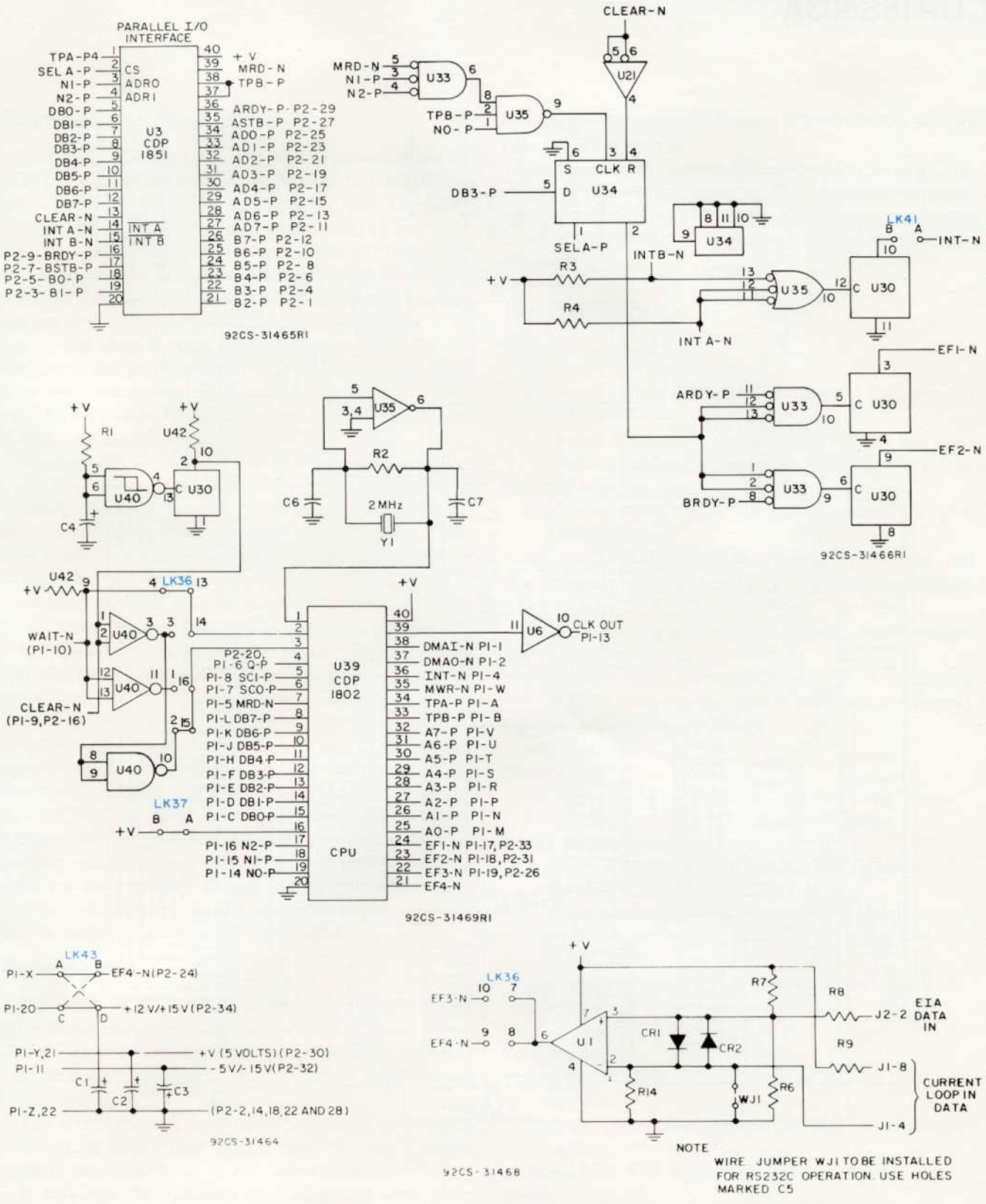

Fig. 5 — Logic Diagram of Microboard Computer CDP18S603A-CPU and Interface Portions.

RCA Microboard Computer
CDP18S603A

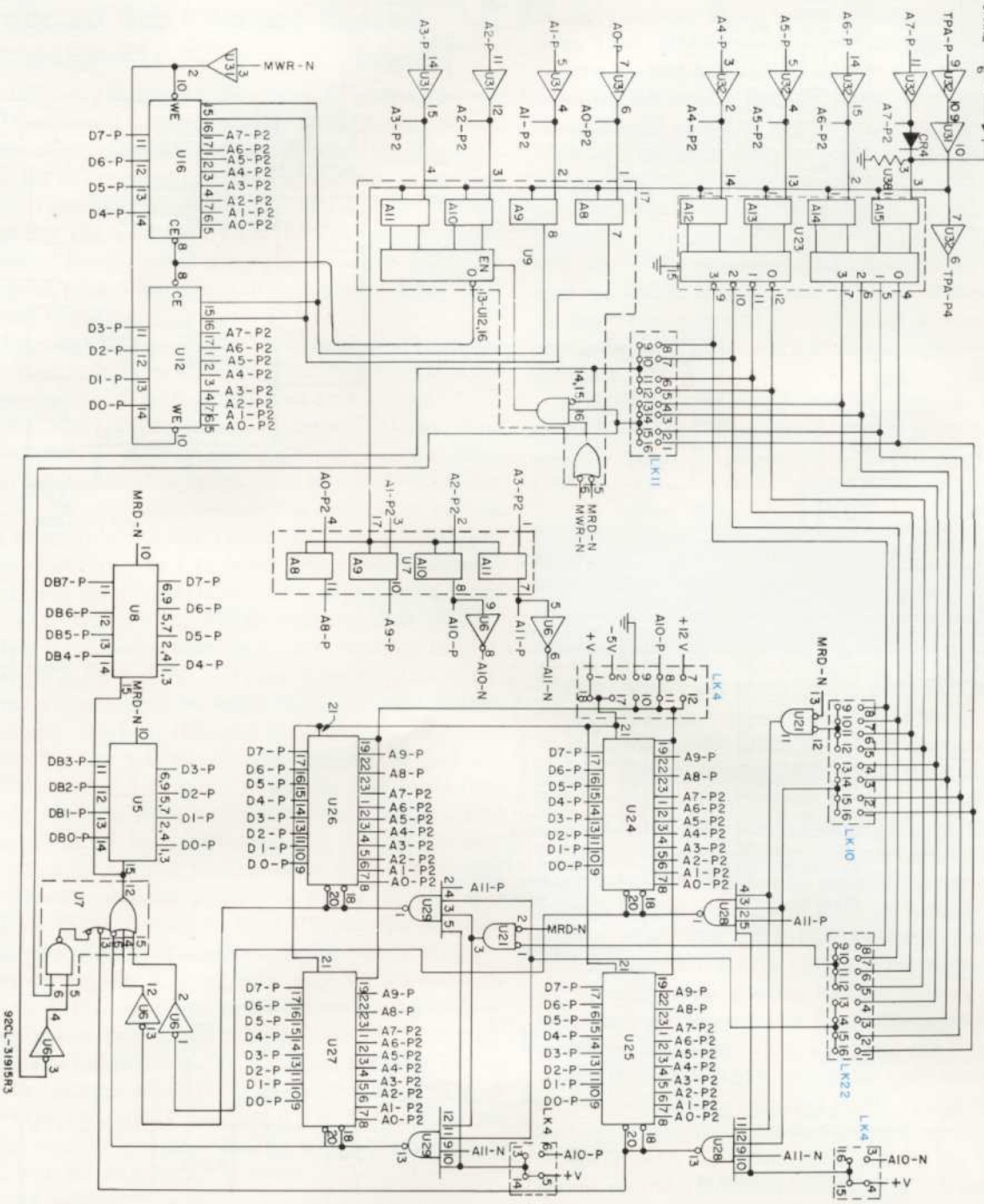

Fig. 4 — Logic Diagram of Microboard Computer CDP18S603A-Memory Portions.

Parts List

C1, C2, C3 = 15μF, 20 V
C4 = 1.5μF 35 V
C6 = 34pF
C7 = 10pF
CR1, CR2, CR3, CR4 = 1N270
J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP 86016-1, keying plug — AMP 87077-1, or equivalent)
P2 mates with a variety of 34-pin flat cable connectors such as T & B Ansley 609-3415M, Berg 65764-005, 3M 3463-0001, or equivalents.
Q1 = 2N5139
R1 = 100 kΩ, ¼ W, 5%
R2 = 22 MΩ, ¼ W, 5%
R3, R4 = 22 kΩ, ¼ W, 5%
R5 = 3 kΩ, ¼ W, 5%
R6, R14 = 1 kΩ, ¼ W, 5%
R7 = 11 kΩ, ¼ W, 5%
R8 = 4.3 kΩ, ¼ W, 5%
R9 = 130 Ω, ¼ W, 5%
R10 = 10 kΩ, ¼ W, 5%
R11 = 2.7 kΩ, ¼ W, 5%
R12 = 100 Ω, ¼ W, 5%
R15-R18 = 22 kΩ, ¼ W, 5%
U1 = CA3160
U2 = CA3140
U3 = CDP1851CE
U5, U8 = CDP1856CE
U6 = CD4069BE
U7 = CDP1867CE
U9 = CDP1866CE
U12, U16 = MWS5114
U20, U38 = resistor module 22 kΩ, 14 pin
U21 = CD4001BE
U23 = CDP1858CE
U28, U29 = CD4012BE
U30 = CD4016BE
U31, U32 = CD4050BE
U33 = CD4025BE
U34 = CD4013BE
U35 = CD4023UBE
U39 = CDP1802CE
U40 = CD4093BE
U42 = resistor module, 22 kΩ, 16 pin
U43 = resistor module SIP, 22 kΩ, 10-pin
U44 = resistor, module SIP, 8-pin
XU3, XU39 = 40-pin socket
XU24-XU27 = 24-pin socket
Y1 = 2.00-MHz crystal

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